Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (Canceled)

17. (Currently Amended) A method of forming an integrated circuit package, comprising:

providing a package housing having a first plurality of bonding pads located on a first bond shelf, the first bond shelf ~~having~~ including a top surface and a first edge;

forming a first conductive strip along the first edge of the first bond shelf, the first conductive strip wrapping around and over the first edge of the first bond shelf to electrically couple ~~from~~ at least one of the first plurality of bonding pads on the first bond shelf to a first conductor under the first bond shelf; and,

removing a portion of the first conductive strip.

18. (Original) The method as recited in claim 17, wherein the first conductive strip is formed by plating a conductive material onto the first edge.

19. (Original) The method as recited in claim 17, wherein the first conductor under the first bond shelf is a power bus.

20. (Original) The method as recited in claim 17, wherein the first conductor under the first bond shelf is a routing trace.

21. (Withdrawn) The method as recited in claim 17, wherein the portion of the first conductive strip is removed by drilling a portion of the first bond shelf.

22. (Withdrawn) The method as recited in claim 21, wherein

the portion drilled in the first bond shelf is a notch.

23. (Withdrawn) The method as recited in claim 17, wherein
the portion of the first conductive strip is removed by
etching away a portion of the first conductive strip of the first bond shelf.

24. (Withdrawn) The method as recited in claim 17, wherein
the package housing is provided by

forming a first conductive layer on a first dielectric substrate,
placing a second dielectric substrate on the first conductive layer of the first dielectric substrate, the second dielectric substrate having a second conductive layer, and
etching the second conductive layer to form the first plurality of bonding pads.

25. (Withdrawn) The method as recited in claim 24, wherein
the first conductive layer forms the first conductor under the first bond shelf.

26. (Withdrawn) The method as recited in claim 24, wherein
the etching of the second conductive layer to further form a second conductor, and
the package housing has a second plurality of bonding pads located on a second bond shelf, the second bond shelf having a second edge, the package housing is further provided by
placing a third dielectric substrate on the second conductive layer of the second dielectric substrate, the third dielectric substrate having a third conductive layer, and
etching the third conductive layer to form a second plurality of bonding pads,
and
the method further includes
forming a second conductive strip along the second edge of the second bond shelf, the second conductive strip wrapping around the second edge of the second bond shelf from at least one of the second plurality of bonding pads on the second bond shelf to the second conductor

under the second bond shelf.

27. (Withdrawn) The method as recited in claim 26, wherein the second conductive layer forms the second conductor under the second bond shelf.

28. (Withdrawn) The method as recited in claim 26, wherein the second conductive strip is formed by plating a conductive material onto the second edge.

29. (Withdrawn) The method as recited in claim 26, wherein the second conductor under the second bond shelf is a power bus.

30. (Withdrawn) The method as recited in claim 26, wherein the second conductor under the second bond shelf is a routing trace.

31. (Original) A method of forming an integrated circuit package, comprising:

providing a package housing having a first bond shelf with a top surface and an inside surface;

forming a conductive material along the inside surface of the first bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the first bond shelf to form at least one of a first plurality of bonding pads on the top surface of the first bond shelf; and,

removing a second portion of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf.

32. (Original) The method as recited in claim 31, wherein the conductive material is formed along the inside surface by plating a conductive material onto the inside surface.

33. (Withdrawn) The method as recited in claim 31, wherein the second portion of the conductive material is removed by drilling a portion of the first

bond shelf.

34. (Withdrawn) The method as recited in claim 33, wherein the portion drilled in the first bond shelf is a notch.

35. (Withdrawn) The method as recited in claim 31, wherein the second portion of the conductive material is removed by etching away a portion of the conductive material from the inside surface of the first bond shelf.

36. (Original) A method of forming an integrated circuit package, comprising:

providing a package housing having a rectangular bond shelf with a rectangular top surface and an inside surface perpendicular with the top surface, the bond shelf having a first plurality of bonding pads located on the top surface;

forming a conductive material along the side surface of the bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the bond shelf to couple to at least one of the first plurality of bonding pads on the top surface of the bond shelf; and,

removing a second portion of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf.

37. (Original) The method as recited in claim 36, wherein the conductive material is formed along the inside surface by plating a conductive material onto the inside surface of the bond shelf.

38. (Withdrawn) The method as recited in claim 36, wherein the second portion of the conductive material is removed by drilling a portion of the bond shelf.

39. (Withdrawn) The method as recited in claim 38, wherein the portion drilled in the bond shelf is a notch.

40. (Withdrawn) The method as recited in claim 36, wherein

the second portion of the conductive material is removed by etching away a portion of the conductive material from the inside of the first bond shelf.